AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A capacitor device, ~~characterized by including~~comprising:

a plurality of electric double-layer capacitors ~~which are~~ connected in series; and

a plurality of balance resistor ~~portion in which~~ portions each comprising m ~~(which is an integer of two or above)~~ resistors ~~having an equivalent resistance are~~ connected in parallel with each other and having equivalent resistance to each other, m being an integer greater than or equal to two;

the plural balance resistor ~~portion~~ portions being connected in parallel to ~~each~~ the plural electric double-layer ~~capacitor~~capacitors, respectively.

2. (Currently Amended) The capacitor device according to claim 1, ~~characterized in that~~ wherein the resistance of at least one of the balance resistor ~~portion~~ portions is equal to, or less than, one-fourth the resistance of each resistor ~~which forms~~ of said at least one of the balance resistor ~~portion~~portions.

3. (Currently Amended) The capacitor device according to claim 1, ~~characterized in that~~ wherein the resistance of at least one of the balance resistor ~~portion~~ portions is equal to, or more than, one-sixth~~, and~~ the resistance of each resistor ~~which forms~~ of said at least one of the balance resistor ~~portion~~portions.

4. (Currently Amended) The capacitor device according to claim 1, ~~characterized in that~~ wherein the resistance of at least one of the balance resistor ~~portion~~ portions is equal to, or more than, one-sixth the resistance of each resistor ~~which forms~~ of said at least one of the balance resistor ~~portion~~ portions and is equal to, or less than, one-fourth ~~this~~ the resistance of each resistor of the at least one of the balance resistor portions.

5. (Currently Amended) The capacitor device according to claim 1, ~~characterized in that~~ wherein the resistance of at least one of the balance resistor ~~portion~~ portions is greater than or equal to 100 Ω or above and less than or equal to 500 Ω ~~or below~~.

6. (Currently Amended) The capacitor device according to claim 1, ~~characterized in that~~ wherein the number of electric double-layer capacitors connected in series is set so that a bias voltage given to each electric double-layer capacitor is lower than the rated voltage of the electric double-layer capacitor.

7. (Currently Amended) The capacitor device according to claim 1, ~~characterized in that~~ wherein one or a plurality of electric double-layer capacitors are further connected in parallel to at least one of the balance resistor ~~portion~~portions.

8. (Currently Amended) A wiring pattern ~~in which a plurality of electric double-layer capacitors are connected in parallel, characterized in that~~comprising:

~~the wiring pattern includes~~ three or more wiring patterns disposed at a predetermined interval;

a plurality of electric double-layer capacitors ~~are~~ connected in parallel between adjacent wiring patterns; and

between two adjacent electric double-layer capacitors which are connected between the wiring patterns, a plurality of resistors, having an equivalent resistance, ~~are~~ connected in parallel to the electric double-layer capacitors.

9. (Currently Amended) The wiring pattern according to claim 8, ~~characterized in that~~ wherein the resistors are connected from one wiring surface of the wiring pattern, and the electric double-layer capacitors are connected from ~~the other~~ another wiring surface of the wiring pattern.